## REMARKS

Claims 1-41 are pending. Claims 1-29 have been allowed; Claims 30 and 32-41 have been rejected; and Claim 31 is objected to. Reconsideration of the rejections and objection is respectfully requested.

*Claim Rejections – 35 U.S.C. § 102*

The Examiner has rejected Claims 30, 35 and 37 under 35 U.S.C. § 102(b) as being anticipated by Sigal (U.S. Patent No. 5,504,441). This rejection is respectfully traversed.

Applicants respectfully submit that Sigal does not teach clock-powered logic as specified in the first line of Claim 30. Clock-powered logic is discussed on page 2 of the present application. The output of a logic stage comprises a clock signal controlled by the input to that stage.

By contrast, Sigal is simply a logic circuit whose timing is governed by clocks whose output is derived from the supply rails in conventional fashion -- see, for example, the source of the OUTPUT signal in Figure 8 of Sigal – it is derived from one of the power rails via gated FETs, not from a gated clock signal.

In consequence, Sigal neither discloses the subject matter of Claim 30 nor can Sigal possibly serve as an effective starting point for an obviousness argument against Claim 30.

Claims 35 and 37 are dependent upon Claim 30 and, for the same reasons, are therefore also not anticipated by Sigal.

*Claim Rejections – 35 U.S.C. § 103*

The Examiner has rejected Claims 32-34 and 36 under 35 U.S.C. § 103(a) as being unpatentable over Sigal in view of Han (UK GB2,248,988). This rejection is respectfully traversed and reconsideration is requested.

Claims 32-34 and 36 are all dependent upon Claim 30. Neither Sigal nor Han, individually or collectively, disclose the features that were discussed above as being missing from Sigal. As a consequence, a *prima facie* case of obviousness has not been made.

The Examiner has rejected Claims 38-41 under 35 U.S.C. § 103(a) being unpatentable over Sigal in view of Dickinson (U.S. Patent No. 5,521,538). This rejection is respectfully traversed and reconsideration is requested.

The Dickinson prior art is not relevant in the putative combination of the Office Action, since Sigal does not even disclose the basic features of Claim 38.

While Dickinson does describe a clock-powered logic circuit, it is of the type identified as prior art in the introduction to the present application. Naturally, this arrangement will suffer from the disadvantages discussed in the introduction to the present application. Dickinson neither discloses nor suggests the non-overlapping clocks defined in Claim 30 (already discussed in the response to the first office action) and so is not relevant as prior art against Claim 30 for either novelty or inventive step.

Claims 39-41 are dependent upon Claim 38 and, for the same reasons, are also viewed as being patentable.

*Objection to Claim 31*

Claim 31 has been objected to as being dependent upon a rejected base claim, but was stated to be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims. As explained above, however, the base claim to Claim 31 should also be allowed. Hence, this objection has been overcome.

## CONCLUSION

For the foregoing reasons, it is respectfully submitted that this case is now in condition for allowance and early notice of the same is earnestly requested.

The Commissioner is authorized to charge Deposit Account No. 501946 for payment of any additional fees required by this response or to credit any overpayment to the account, and include attorney reference no. 61450-023-6806. A duplicate copy of this sheet is enclosed.

Respectfully,
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